CLAIMS

What is claimed is:

1. A method, comprising:

executing an instruction that updates data in a register at a first time;

marking the instruction as a slowable instruction when the data is not read from the register at a next clock cycle from completion of execution of the instruction.

2. The method of claim 1, further comprising:

storing an instruction address of the instruction.

3. The method of claim 2, further comprising:

when the instruction is marked as a slowable instruction, using the stored instruction address to store an entry indicating that the instruction is slowable.

4. The method of claim 3, further comprising;

when the instruction address of the instruction is encountered a second time and the instruction is marked as a slowable instruction, delaying processing of the instruction.

5. The method of claim 4, wherein when the instruction address of the instruction is encountered the second time, the stored entry is used to determine if the instruction is slowable.

6. The method of claim 4, wherein delaying the processing of the instruction comprises delaying decoding the instruction.

7. The method of claim 4, wherein delaying the processing of the instruction comprises using lower priority resources to execute the instruction.

8. The method of claim 4, wherein delaying the processing of the instruction comprises delaying loading the data into the register until prior to the data is read from the register.

9. A method, comprising:

recording a first clock cycle when an instruction that loads data into a register is to complete;

recording a second clock cycle when the data is read from the register; and

making the instruction as a slowable instruction when the second clock cycle is more than a predetermined time threshold from the first clock cycle.

10. The method of claim 9, wherein the predetermined time threshold is at least one clock cycle.

11. The method of claim 9, further comprising:

storing an instruction address of the instruction at a first time.

12. The method of claim 11, further comprising:

when the instruction is marked as a slowable instruction, using the stored instruction address to store an entry indicating that the instruction is slowable.

13. The method of claim 12, wherein when the instruction address of the instruction is loaded into an instruction pointer at a second time, the stored entry is used to determine if the instruction is slowable.

14. The method of claim 13, wherein when the instruction is determined to be slowable, processing of the instruction is delayed.

15. The method of claim 14, wherein the processing of the instruction is delayed by delaying decoding the instruction.

16. The method of claim 14, wherein the processing of the instruction is delayed by using lower priority resources to execute the instruction.

17. The method of claim 9, wherein information about the first clock cycle and the second clock cycle is provided by a scheduler.

18. The method of claim 17, wherein the scheduler provides the information about the first clock cycle and the second clock cycle prior to execution of the instruction.

19. A computer readable medium having stored thereon sequences of instructions which are executable by a system, and which, when executed by the system, cause the system to perform a method, comprising:

executing an instruction that loads data into a register at a first time; and

marking the instruction as a slowable instruction when the data is not read from the register at a next clock cycle from completion of execution of the instruction.

20. The computer readable medium of claim 19, further comprising:

storing an instruction address of the instruction.

21. The computer readable medium of claim 20, further comprising:

when the instruction is marked as a slowable instruction, using the stored instruction address to store an entry indicating the instruction is slowable.

22. The computer readable medium of claim 21, further comprising; when the instruction address of the instruction is encountered a second time and the instruction is marked as a slowable instruction, delaying processing of the instruction.

23. The computer readable medium of claim 22, wherein when the instruction address of the instruction is encountered the second time, the stored entry is used to determine if the instruction is marked as a slowable instruction.

24. The computer readable medium of claim 22, wherein delaying the processing of the instruction comprises delaying decoding the instruction.

25. The computer readable medium of claim 22, wherein delaying the processing of the instruction comprises using lower priority resources to execute the instruction.

26. The computer readable medium of claim 22, wherein delaying the processing of the instruction comprises delaying loading the data into the register until prior to the data is read from the register.

27. A computer readable medium having stored thereon sequences of instructions which are executable by a system, and which, when executed by the system, cause the system to perform a method, comprising:

recording a first clock cycle when an instruction is to complete loading data in a register;

recording a second clock cycle when the data is read from the register; and

making the instruction as a slowable instruction when the second clock cycle is more than a predetermined time threshold from the first clock cycle.

28. The computer readable medium of claim 27, wherein the predetermined time threshold is at least one clock cycle.

29. The computer readable medium of claim 27, further comprising:

storing an instruction address of the instruction at a first time.

30. The computer readable medium of claim 29, further comprising:

when the instruction is marked as a slowable instruction, using the stored instruction address to store an entry indicating that the instruction is a slowable instruction.

31. The computer readable medium of claim 30, wherein when the instruction address of the instruction is loaded into an instruction pointer at a second time, the stored entry is used to determine if the instruction is a slowable instruction.

32. The computer readable medium of claim 31, wherein when the instruction is determined to be slowable, processing of the instruction is delayed.

33. The computer readable medium of claim 32, wherein the processing of the instruction is delayed by delaying decoding the instruction.

34. The computer readable medium of claim 32, wherein the processing of the instruction is delayed by using lower priority resources to execute the instruction.

35. The computer readable medium of claim 27, wherein information about the first clock cycle and the second clock cycle are provided by a scheduler.

36. The computer readable medium of claim 35, wherein the scheduler provides the information about the first clock cycle and the second clock cycle prior to execution of the instruction.

37. A system, comprising:

a processor;

a memory coupled with the processor; and

a register file coupled with the memory and the processor, wherein each of a plurality of registers in the register file is associated with an instruction address of an instruction that loads data into the register.

38. The system of claim 37, wherein each of the plurality of registers in the register file is associated with a state, the state indicating whether the instruction that loads data into the register is a slowable instruction or a non-slowable instruction.

39. The system of claim 38, wherein after the data is loaded into the register by the instruction and the data is not read from the register in a next clock cycle, the state associated with the register is updated to indicate that the instruction is a slowable instruction.

40. The system of claim 39, wherein when the instruction is indicated to be a slowable instruction, a history file is updated to indicate that the instruction is a slowable instruction.

41. The system of claim 40, wherein the history file is updated using the instruction address of the instruction.

42. The system of claim 37, wherein each of the plurality of registers in the register file is associated with a write time stamp (WTS) to indicate a time when data is written into the register, a read time stamp (RTS) to indicate a time when the data is read from the register, and a read state to indicate if the data is read from the register within a predetermined number of clock cycles.

43. The system of claim 42, wherein when the data is not read from the register within the predetermined number of clock cycles, the instruction that loads the data into the register at the time indicated by the write time stamp is identified as a slowable instruction.

44. The system of claim 43, wherein when the instruction is identified as a slowable instruction, a history file is updated to indicate that the instruction is a slowable instruction.

45. The system of claim 44, wherein the history file is updated using the instruction address of the instruction.

46. The system of claim 45, wherein the history file is used to identify that the instruction is the slowable instruction when the instruction address of the instruction is loaded into an instruction pointer register.

47. The system of claim 42, wherein the WTS and the RTS are provided by an instruction scheduler.